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(54) Charge coupled image sensor with u-shaped gates

(57) A method and apparatus of forming adjacent, non-overlapping CCD electrodes within an image sensing device such that the electrodes are U-shaped. The device provided by the disclosed method employs a substrate with a gate dielectric layer formed on a surface of the substrate with a plurality of phases created within the CCD. A deposited silicon layer is placed on the surface of the CCD and a mask is used to cover areas other than the first set of electrodes. Etching takes place

leaving the mask areas to the deposited silicon and a set of side walls to the remaining deposited silicon are then oxidized. A first set of electrodes by forming an electrode layer placed over the CCD. CMP is employed to remove remaining deposited silicon layer as well as portions of the electrode layer such that the side walls remain vertical portions to electrode layer remaining in the side walls. The process is then repeated by placing another electrode material layer and another CMP process leaving two sets of adjacent U-shaped gates.

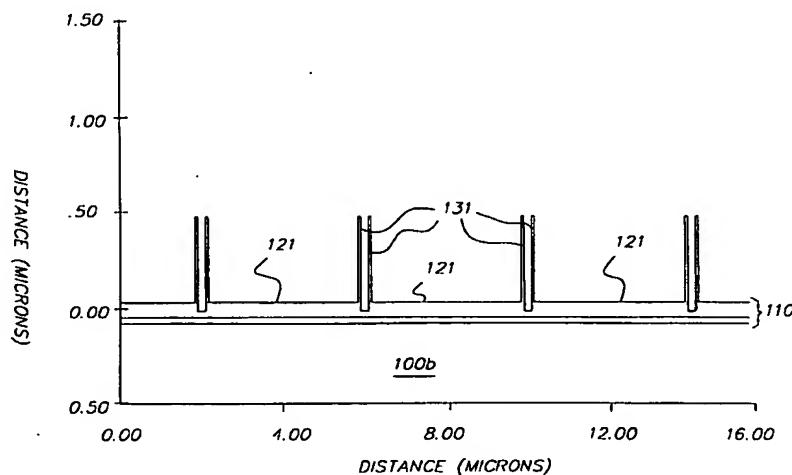


FIG. 1c

Description

[0001] The present invention relates to the formation of electrodes within charge coupled devices, and more particularly, to the formation of nonoverlapping electrodes within charge coupled devices.

[0002] Solid state image sensors are very commonly based charge coupled device (CCD) technology, and are generally classified into either interline transfer type or frame transfer type. The CCD image sensing device is typically an array of closely spaced gates composed of polycrystalline silicon (polysilicon). Polysilicon has been a material of choice due to the ease with which a reliable thin insulating layer may be produced to insulate the separate gates from one another. In operation of frame transfer type imagers, incident light must pass through the gate electrodes and be absorbed by the underlying silicon. Thus, it is desired that these gates be transparent to a broad spectrum of wavelengths of light, and in particular to be transparent to shorter wavelengths, for example, shorter than 450 nm wavelength. Polysilicon gates are not suitable for high transmission in this wavelength range. Hence, devices utilizing more transparent conducting materials, typically composed of conducting oxide materials such as indium-tin-oxide (ITO), have been proposed. For purposes of this disclosure, the term ITO is to be understood to include other conducting materials, as well.

[0003] In the prior art as taught by Losee, in U.S. Patent No. 5,891,752, a method for constructing a CCD image sensor with all ITO gates is proposed. In that device, however, the ITO gates are subjected to chemical mechanical polishing (CMP) to achieve the required electrical isolation between adjacent gates. This CMP process can be non-uniform over widely spaced regions and, hence, devices so produced have some variation in ITO thickness from one area of the device to another. Due to the relatively high index of refraction of the ITO material, this thickness variation results in variation in the relative amount of light which reaches the silicon substrate, and hence, produces a spatial variation in the relative sensitivity of the device. For improved optical response, it is desirable to employ relatively thin ITO for the gates, for example, using thicknesses less than 100 nm. With decreasing ITO gate thickness, the variation in thickness caused by the CMP process causes stronger variation in the relative sensitivity of the device.

[0004] Another concern with the polished structure, particularly when thin ITO gates are desired, is due to fixed electrostatic charges which inevitably occur in overlying insulating layers of the device. Such fixed charge will cause small potential variations, usually as regions of increased electrostatic potential, immediately below the insulating gap between the CCD electrodes. This is illustrated in Fig. 1a. In this figure, electrostatic potential contours are indicated, and it is seen that a potential well, or pocket, appears in the region beneath the electrode gap. The depth of this well depends on both

the gate electrode separation and the placement and magnitude of the fixed insulator charge. Such a potential well can introduce charge transfer inefficiency, an undesirable property, in the operation of the CCD shift register.

[0005] From the foregoing it should be apparent that there remains a need in the art for a method of producing a more uniform gate thickness in frame transfer CCD images sensors, this is especially true when the gates are composed of ITO. It should also be apparent that there remains a problem of reducing the effect of fixed charges which may be present in overlying insulating layers. Such fixed charges can result in undesirable potential wells or barriers in the underlying silicon substrate, which, in turn, can lead to charge transfer inefficiency. These and other problems within the prior art are addressed by the present invention.

[0006] The present invention addresses the problem of producing a more uniform gate thickness in frame transfer CCD images sensors with all gates composed of ITO. It also addresses the problem of reducing the effect of fixed charges which may be present in overlying insulating layers. Such fixed charges can result in undesirable potential wells or barriers in the underlying silicon substrate, which, in turn, can lead to charge transfer inefficiency. A device and method of manufacture are disclosed wherein the gate electrodes are of a substantially U-shaped geometry, which effectively shields the charge transfer channel from the effects of the fixed charge and wherein the gate electrode material, for example, ITO, is of improved optical uniformity.

[0007] The present invention discloses a CCD based image sensing device with non-overlapping gates wherein the gates have a vertical conducting section at their edges. With such vertical edge sections present, the deleterious effects of the fixed insulator charges in the upper layers of the CCD are electrostatically shielded, such shielding resulting in a reduced channel potential well between the gates. Such a shielding effect is shown in the calculated potential profile of the CCD channel in Fig. 1a and Fig. 1b. In Fig. 1a, the gate electrode thickness is thinner than the space between the electrodes. For purposes of this illustration, the voltages on the two gates in the figure are equal. It is seen that a potential non-uniformity exists in the gap between the gate electrodes. This is indicated by the presence of the oval shaped contour in the center of the figure. In Fig. 1b, the gate electrodes are provided with vertical edge regions which act to partially shield the substrate from the effect of the fixed charge and the potential well is reduced.

Comparing Fig. 1b with Fig. 1a, the gate electrode thickness remains the same as in Fig. 1a, and thus the optical characteristics are substantially the same for the two devices. The general form of the gate structure, in cross-section, with such vertical edges is thus U-shaped. In Fig. 1c, a more extended cross-sectional diagram of a CCD structure is shown.

[0008] The present invention has the advantage that

a CMP process does not touch the horizontal surfaces of ITO gates (polysilicon) which in turn eliminates non-uniformity in the gate that typically results from the CMP process. The present invention provides vertical sections between the individual gates which act as an electrostatic shield resulting in only small potential wells occurring between the gates. This also simplifies the polishing process. These advantages are obtained without requiring any additional steps.

Fig. 1a is a potential contour map for a prior art device with thin gate electrodes illustrating the gap between electrode gates and the resulting ;

Fig. 1b is a potential contours with vertical extensions on gates;

Fig. 1c is a completed CCD structure where gates are non-overlapping and have vertical conductive sections at gate edges (U-shaped structure); and Figs. 2a-2i is a process flow and simulation chart outlining a method of fabrication of a CCD with such U-shaped gates.

[0009] Fig. 1a shows equipotential contours calculated from the electrostatic modeling of a region of a CCD device wherein gate electrodes, 105a and 106a are non-overlapping and are separated from each other by a gap, 101a, the gap, of width w, being greater than the thickness, t, of the gate electrodes. The gate electrodes are separated from the semiconductor substrate, 100a, by a gate dielectric, 110a. The semiconductor substrate, 100a, is provided with doping to produce a buried channel CCD device as is well understood by those skilled in the art. It is seen that the gap, 101a, produces a region of increased potential, 115a, in the substrate. The magnitude of the potential non-uniformity is dependent on the gap width as well as any fixed charge which might be present in the layers above the gap. The presence of such potential non-uniformities is deleterious to the efficient transfer of charge in the CCD and, therefore, should be minimized.

[0010] In Fig. 1b, the gate electrodes, 105b and 106b, are separated from semiconductor 100b by dielectric 110b and the gate electrodes, 105b and 106b, are separated by gap, 101b, of width w, with the additional feature that the edges of the electrodes are extended vertically to include vertical electrode segments, 107 and 108. Again, equipotential contours are calculated by electrostatic modeling. In this case, by contrast with Fig. 1a, it is seen that the potential non-uniformity, 115b, in the region below the gap is reduced. This is due to the shielding effect of the vertical segments, 107 and 108.

[0011] Fig. 1c shows, schematically, a cross-section of a portion of a CCD shift register wherein each gate consists of horizontal sections 121 and vertical edge sections 131. As is well known, the semiconductor substrate for such an array of such gates may be provided with dopants and the gates are connected to clocking voltages to effect the charge transfer.

[0012] It has been discovered that a CCD based image sensing device with non-overlapping gates can be provided wherein the gates have a vertical conducting section at their edges. The vertical edge sections prevent the deleterious effects of the fixed insulator charges in the upper layers of the CCD which are electrostatically shielded. The shielding results in a reduced channel potential well between the gates. Such a shielding effect is shown in the calculated potential profile of the CCD channel in Fig. 1a and Fig. 1b. In Fig. 1a, the gate electrode thickness is thinner than the space between the electrodes. For purposes of this illustration, the voltages on the two gates in the figure are equal. It is seen that a potential non-uniformity exists in the gap between the gate electrodes. This is indicated by the presence of the oval shaped contour in the center of the figure. In Fig. 1b, the gate electrodes are provided with vertical edge regions which act to partially shield the substrate from the effect of the fixed charge and the potential well is reduced. Comparing Fig. 1b with Fig. 1a, the gate electrode thickness remains the same as in Fig. 1a, and thus the optical characteristics are substantially the same for the two devices. The general form of the gate structure, in cross-section, with such vertical edges is thus U-shaped. In Fig. 1c, a more extended cross-sectional diagram of a CCD structure is shown.

[0013] Referring to Figs. 2a-2i, the method of fabrication of a charge coupled device (CCD) having U-shaped electrode gates is outlined. Referring now to Fig. 2a, a silicon substrate 12 is covered with a dielectric layer 14. The gate dielectric layer 14 is a bilayer stack of silicon oxide and silicon nitride in the preferred embodiment. However, it will be readily apparent to those skilled in the art, that other materials can also be used for the dielectric layer 14. Still referring to Fig. 2a, a plurality of phases within the CCD 10 are formed by depositing a silicon layer 16 on the surface of the CCD 10 and forming a Chemical Mechanical Polishing (CMP) polish stop layer 18 on the deposited silicon layer 16. The CMP polish stop layer 18 is preferably a nitride material. Both the deposited silicon layer 16 and the CMP polish stop layer 18 are then photolithographically etched to the open areas 17 within the phases where electrodes are to be formed.

[0014] Referring to Fig. 2b, the photolithographically etched deposited silicon layer 16 areas are then oxidized to create side walls 21 on the remaining areas of the deposited silicon layer 16. The preferred embodiment of the present invention envisions a two-phase charge coupled device. In order to facilitate the charge transfer within a two-phase charge transfer device, barrier implants are necessary to control the direction of charge transfer. Thus, referring to Fig. 2c, photoresist 23 is formed on the CCD 10 as such that the areas where barrier implants 25 are desired are exposed. In the present invention a boron implant is envisioned, but other types of implants are specifically envisioned also, both p-type and n-type. After the implants 25 are formed,

the photoresist 23 is stripped and the CCD is annealed. [0015] Referring now to Fig. 2d, a gate electrode material 32 is deposited over the CCD 10. Here, the gate electrode material 32 is formed over the oxidized side walls 21 such that the formed gate electrode layer 32 has both horizontal and vertical components. A polish buffer layer 34 is then placed over the gate electrode material 32. A low temperature oxide (LTO) is preferred as the polish buffer layer 34. In the preferred embodiment ITO is used as gate electrode material 32 because of its transparency, especially in the blue wavelengths. Also, it is specifically envisioned the polysilicon can be used as the gate electrode material 32. Also, materials can be used that selectively result in specific transparency bandwidths.

[0016] Referring to Fig. 2e, the polish buffer layer 34 is removed via chemical mechanical polishing down through the gate electrode material 32 to the CMP polish stop layer 18. This leaves a vertical component layer 35 of gate electrode material 32 on the oxidized side walls 21 in a vertical direction as well as a horizontal component layer 36 to the gate electrode material 32.

[0017] Referring to Fig. 2f, the material used to form the CMP polish stop layer 18 is removed along with the unoxidized portion of the deposited silicon layer 16. This removal is typically accomplished by subjecting the structure to an etchant, either a plasma etch or a liquid chemical etch, which will remove the polish stop material but will not significantly attack other exposed materials. This polish stop removal is followed by a second etch of the then exposed silicon layer 16, where the silicon etchant does not substantially attack the remaining exposed materials. Appropriate etchants may be selected as are well known to those experienced in the art. For example, for a polish stop layer composed of silicon nitride, a fluorine containing plasma etch may be used to effectively remove the nitride but leaving the oxide and ITO layers intact. This is then followed by a chlorine containing plasma etch which removes the exposed silicon but leaves the ITO and the oxide intact.

[0018] Fig. 2g illustrates the process of creating the next set of phases to CCD 10 by placement of a photoresist layer 43 to provide a mask for another barrier implant 45. The photoresist layer 43 is then stripped and referring to Fig. 2h, a second gate electrode material 52 is applied to the CCD 10. Another polish buffer layer 54 which again is a low temperature oxide (LTO) is then placed on the CCD 10 which creates a set of protrusions 58 over side wall 21.

[0019] Referring to Fig. 2i, the polish buffer layer 54 is removed via chemical mechanical polishing down through the protrusion 58 so that both layers of gate electrode material 32, 52 form U-shaped gates 61, 62 with now defined first and second phases 1, 2 of CCD 10. This leaves a vertical component layer 55 of gate electrode material 52 on the oxidized side walls 21 in a vertical direction as well as a horizontal component layer 56 to the gate electrode material 52.

[0020] The preferred embodiment to the present invention is provided with doped regions and insulating regions in such a way that an array of separated photo-sensitive sites, or pixels, is defined. Charge transfer channels are provided as a part of this array. An insulating layer, gate dielectric, is provided over the charge transfer channel. This insulating layer may be composed of one or more separate insulating layers; for example, silicon dioxide (oxide) and silicon nitride. Vertical insulating spacers are provided, for example, by the method suggested in Fig. 1a through Fig. 1e in U.S. Patent No. 5,891,752.

15 Claims

1. A charge coupled device having adjacent, closely spaced, non-overlapping gates comprising:
20 a semiconductor substrate having a gate dielectric layer formed on a surface;
a plurality of phases within the CCD wherein each of the phases has an electrode;
25 an insulating material interspersed between the gates; and
a gate electrode material formed in the electrodes such that the gate electrode material has a substantially horizontal part and a substantially vertical part, with the vertical part adjacent to the interspersed insulating material, the vertical part extending a distance above the horizontal part.
2. The charge coupled device defined in as in claim 1,
35 wherein the gate conductors further comprise indium tin oxide (ITO).
3. The charge coupled device defined in as in claim 1,
40 wherein the gate conductors further comprise polysilicon.
4. A charge coupled device of claim 1 wherein the plurality of phases result in a two-phase charge coupled device with implants formed within the phases.
5. A charge coupled device as in claim 1, wherein the horizontal parts of the gate electrode material are
45 of substantially identical thickness.
6. A method of forming CCD electrodes within an image sensing device comprising the steps of:
50 providing a substrate with a gate dielectric layer formed on a surface;
55 creating a plurality of phases within the CCD by forming a first set of electrodes by forming a deposited silicon layer on the surface of the CCD; forming a CMP polish stop layer on the depos-

ited silicon layer;
removing the deposited layer from areas where
the first set of electrodes is to be formed;
oxidizing the side walls of the remaining depos-
ited silicon layer; 5
depositing a gate electrode material on the
CCD and a polish buffer layer on the gate elec-
trode material;
polishing the device until the gate electrode ma-
terial is removed from the areas above the 10
polish stop layer and the deposited silicon;
removing the polish stop layer and the unoxi-
dized portion of the deposited silicon layer;
depositing a second layer of gate electrode ma-
terial on the device and a second polish buffer 15
layer on the second gate electrode material;
and
polishing the device until there is no second
gate electrode material either on top of or in
contact with the first gate electrode material. 20

7. The method of claim 6 wherein the CCD is a two-
phase CCD and implants are created prior the steps
of depositing the gate electrode material. 25
8. The method of claim 6 wherein the providing step
further comprises the gate dielectric layer to be ox-
idation resistant.
9. The method of claim 6 wherein the providing step 30
further comprises the gate dielectric layer is a bilay-
er stack of silicon oxide and silicon nitride.
10. The method of claim 6 wherein the deposited silicon
layer is either amorphous or crystalline. 35

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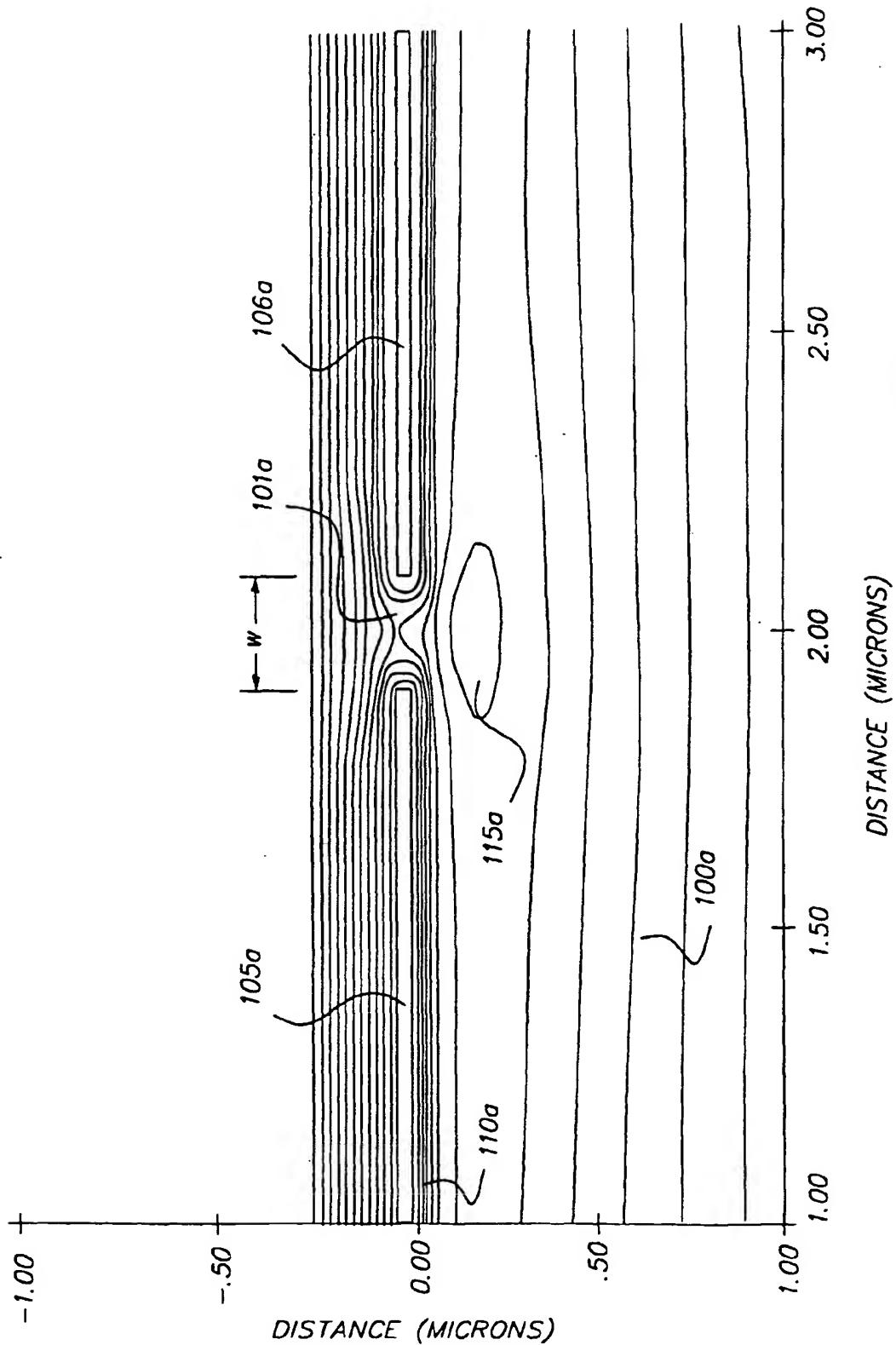


FIG. 1a

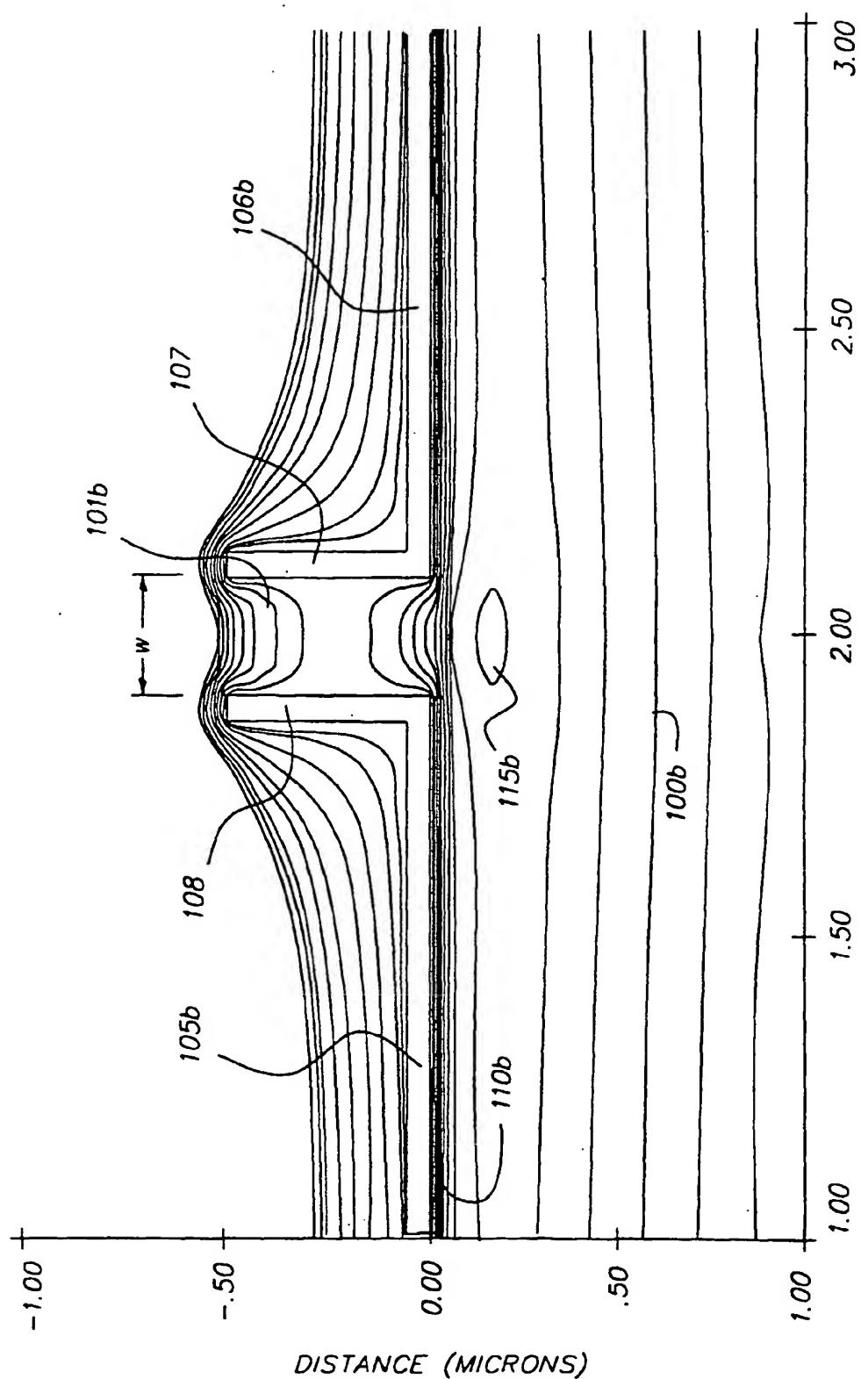


FIG. 1b

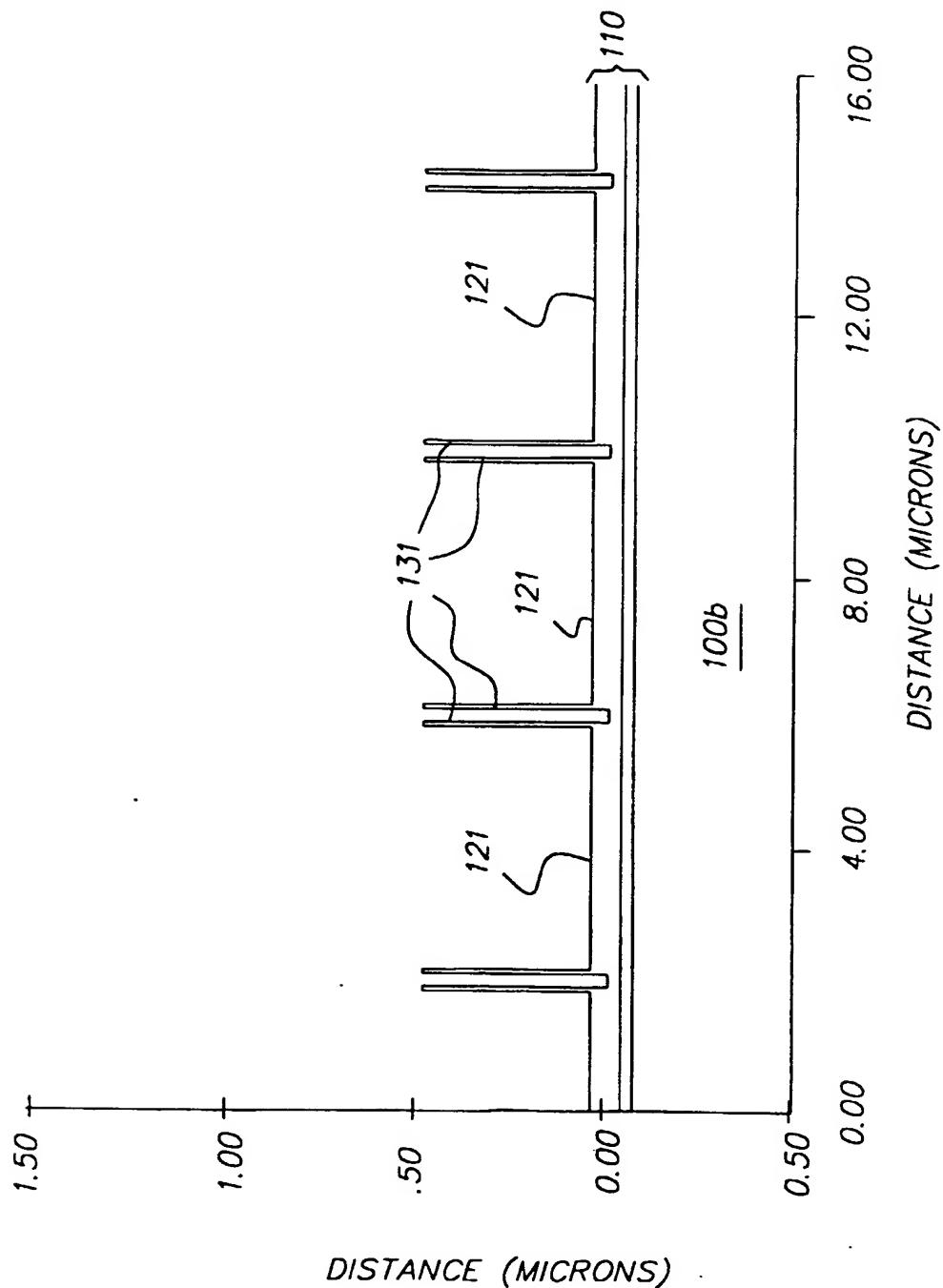


FIG. 1c

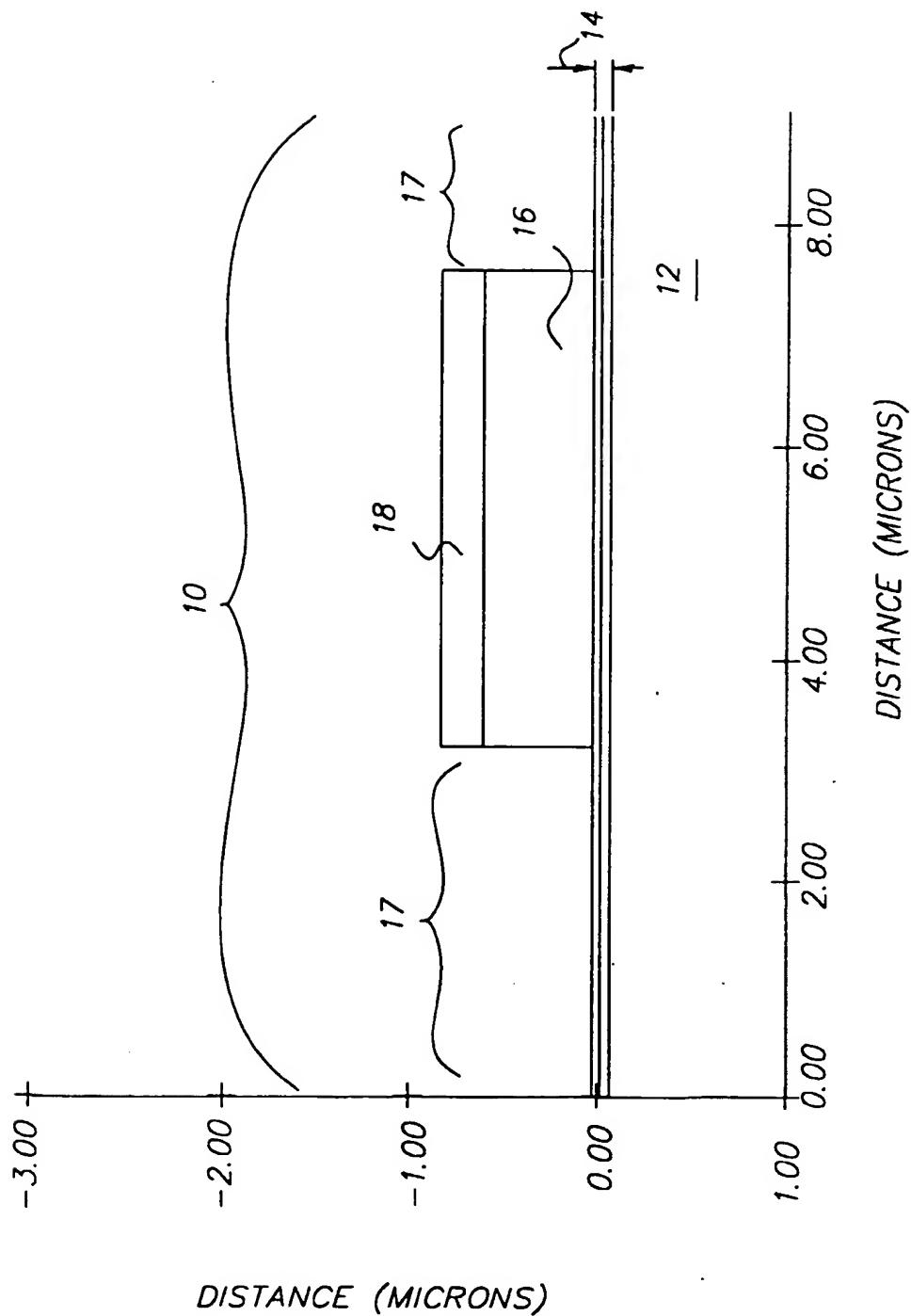


FIG. 2a

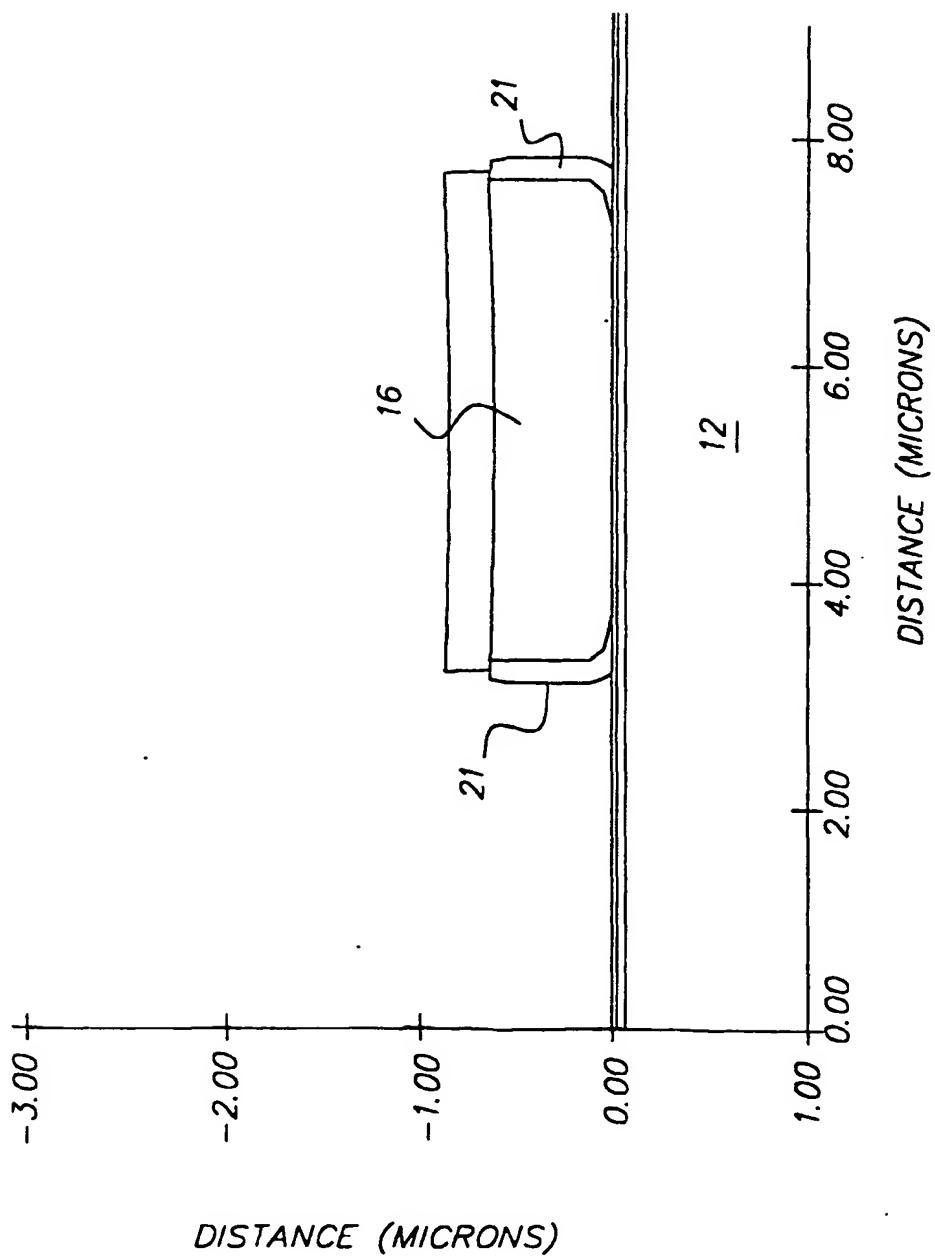


FIG. 2b

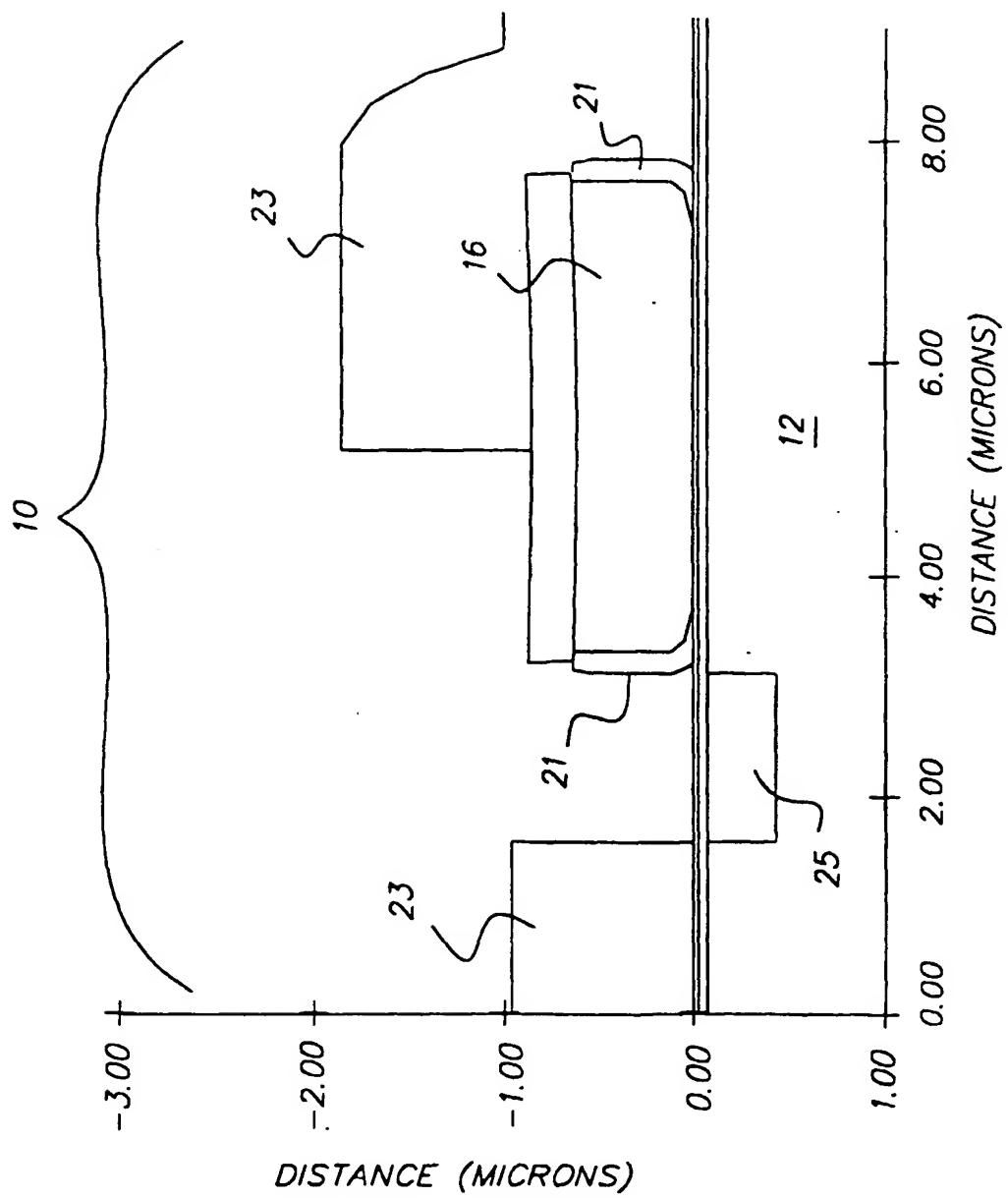


FIG. 2c

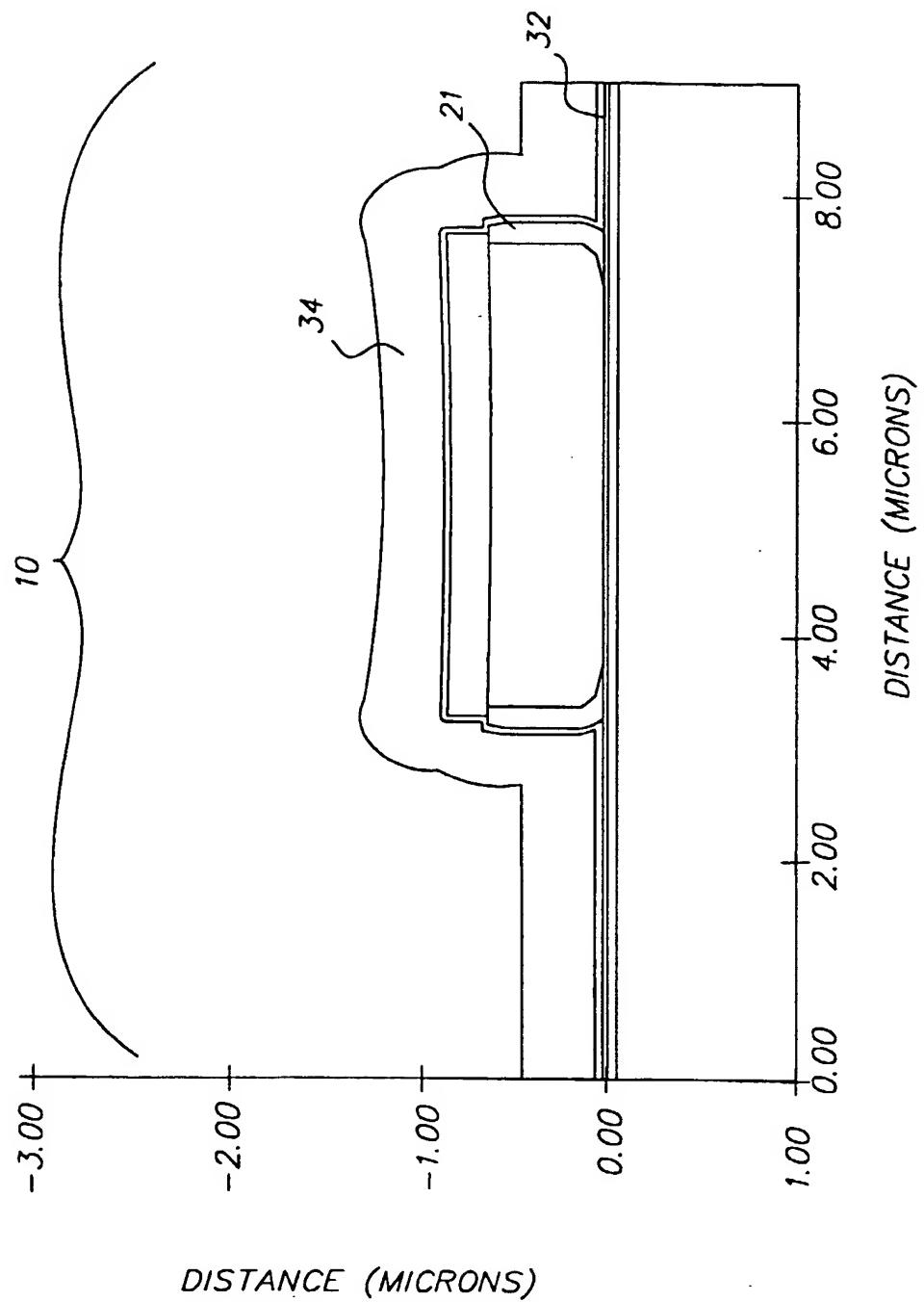


FIG. 2d

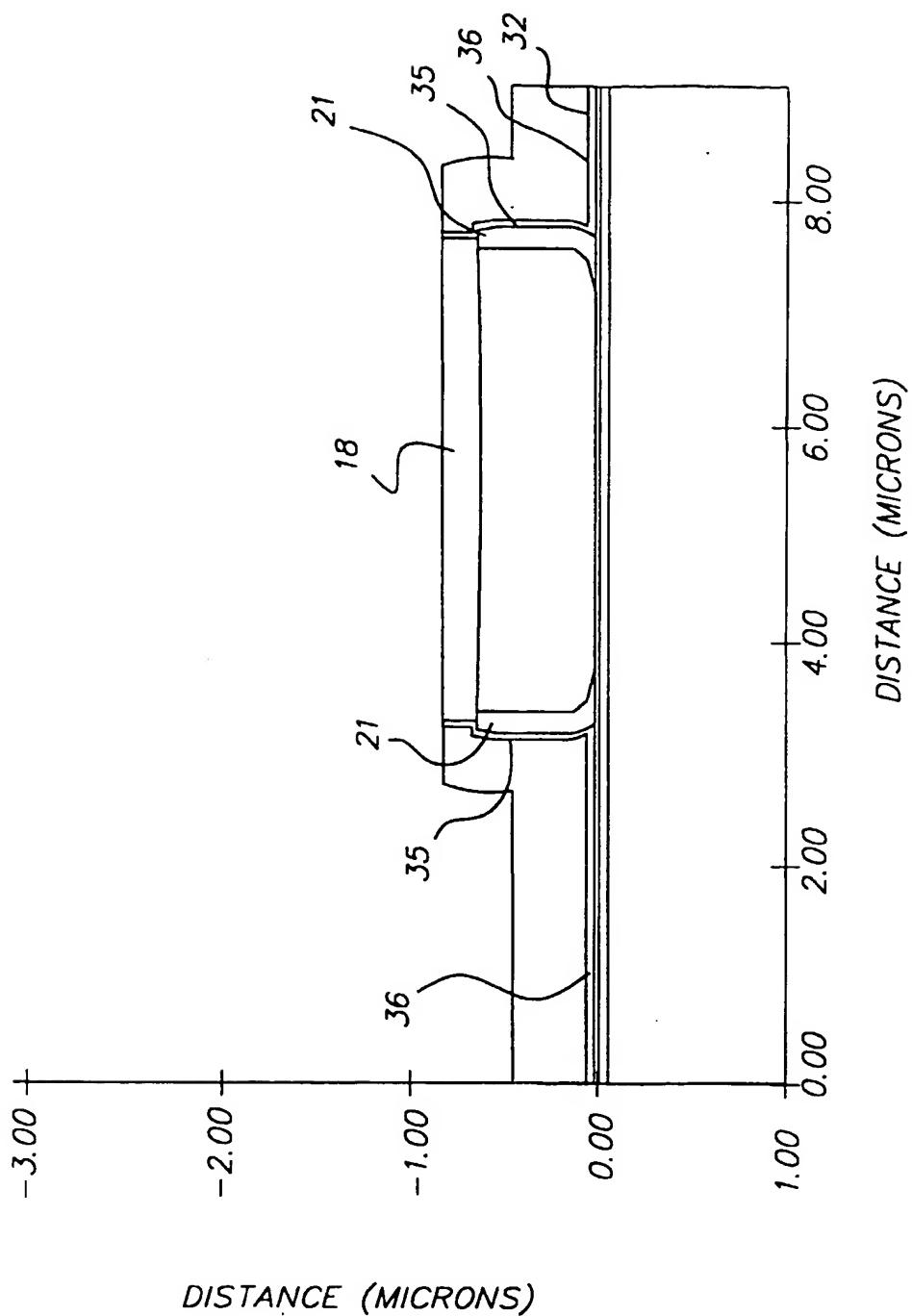


FIG. 2e

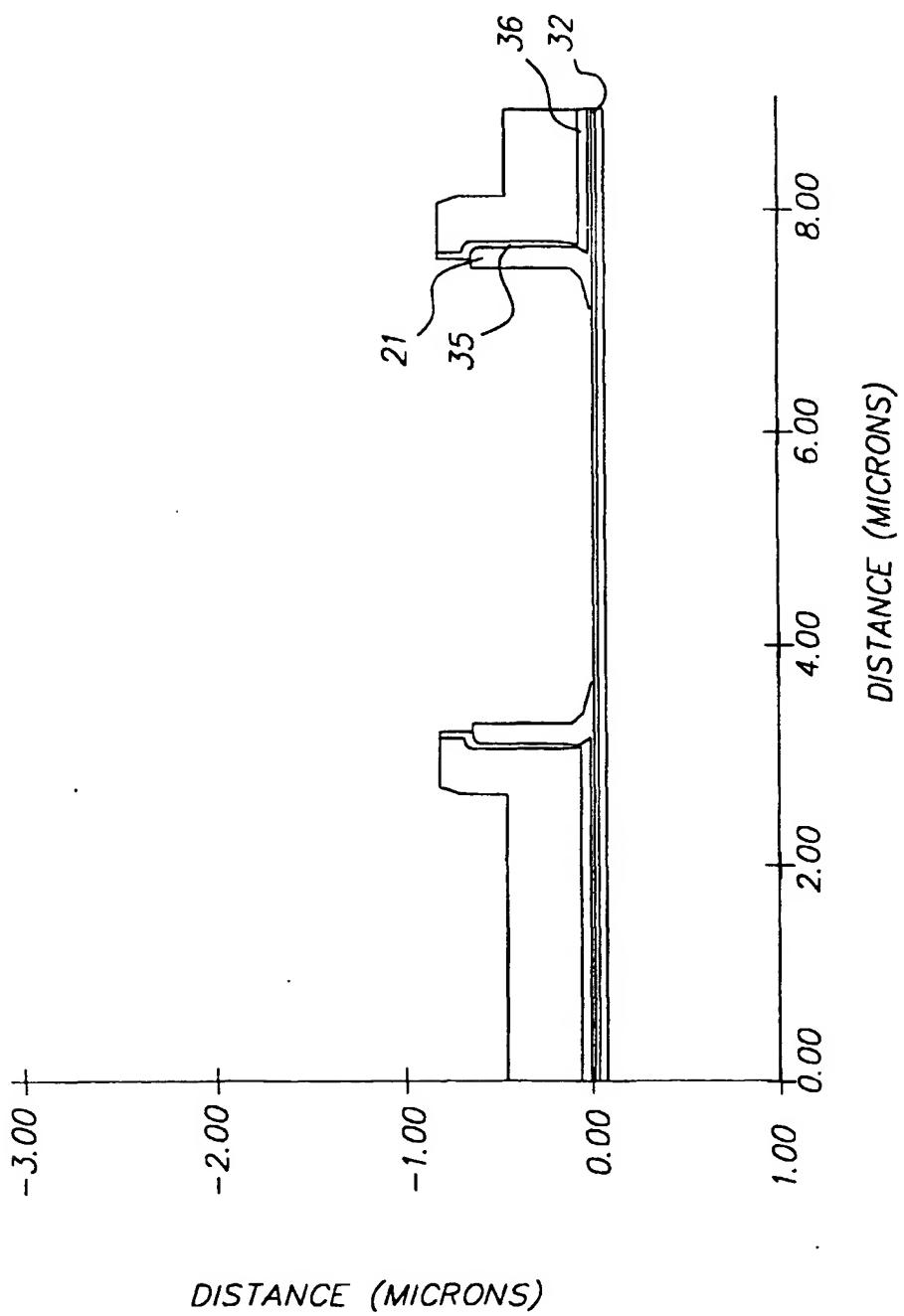


FIG. 2f

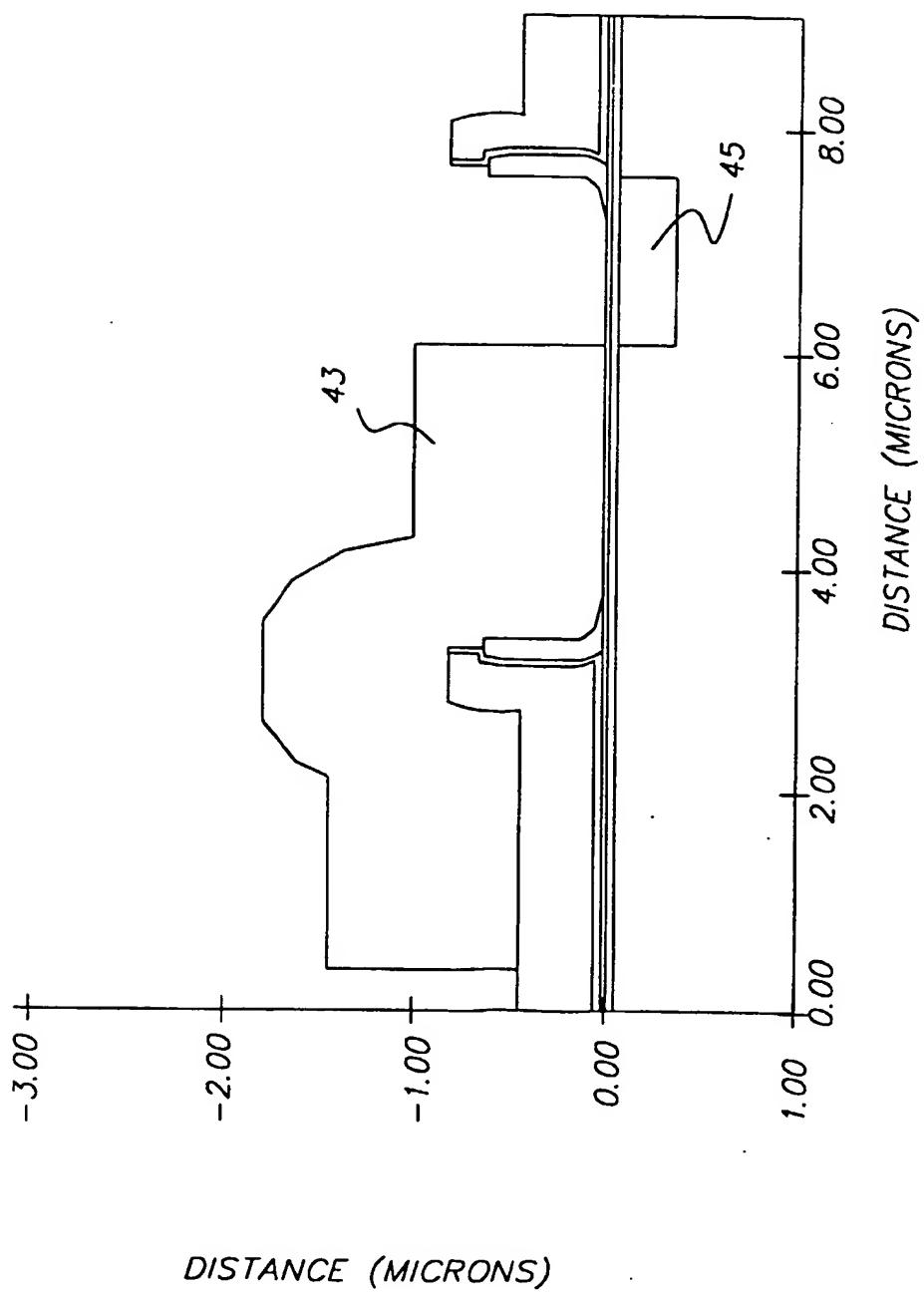


FIG. 2g

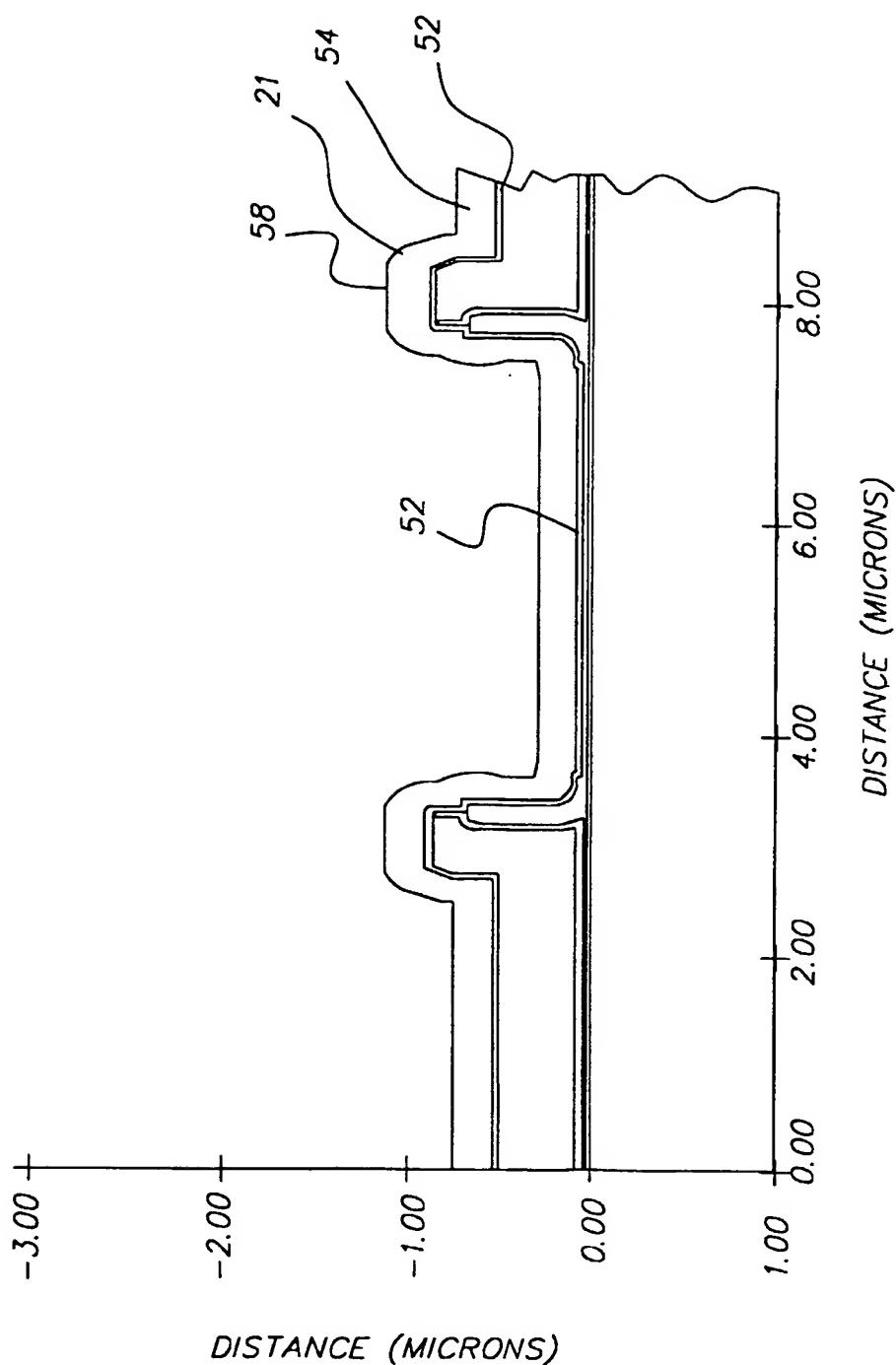


FIG. 2h

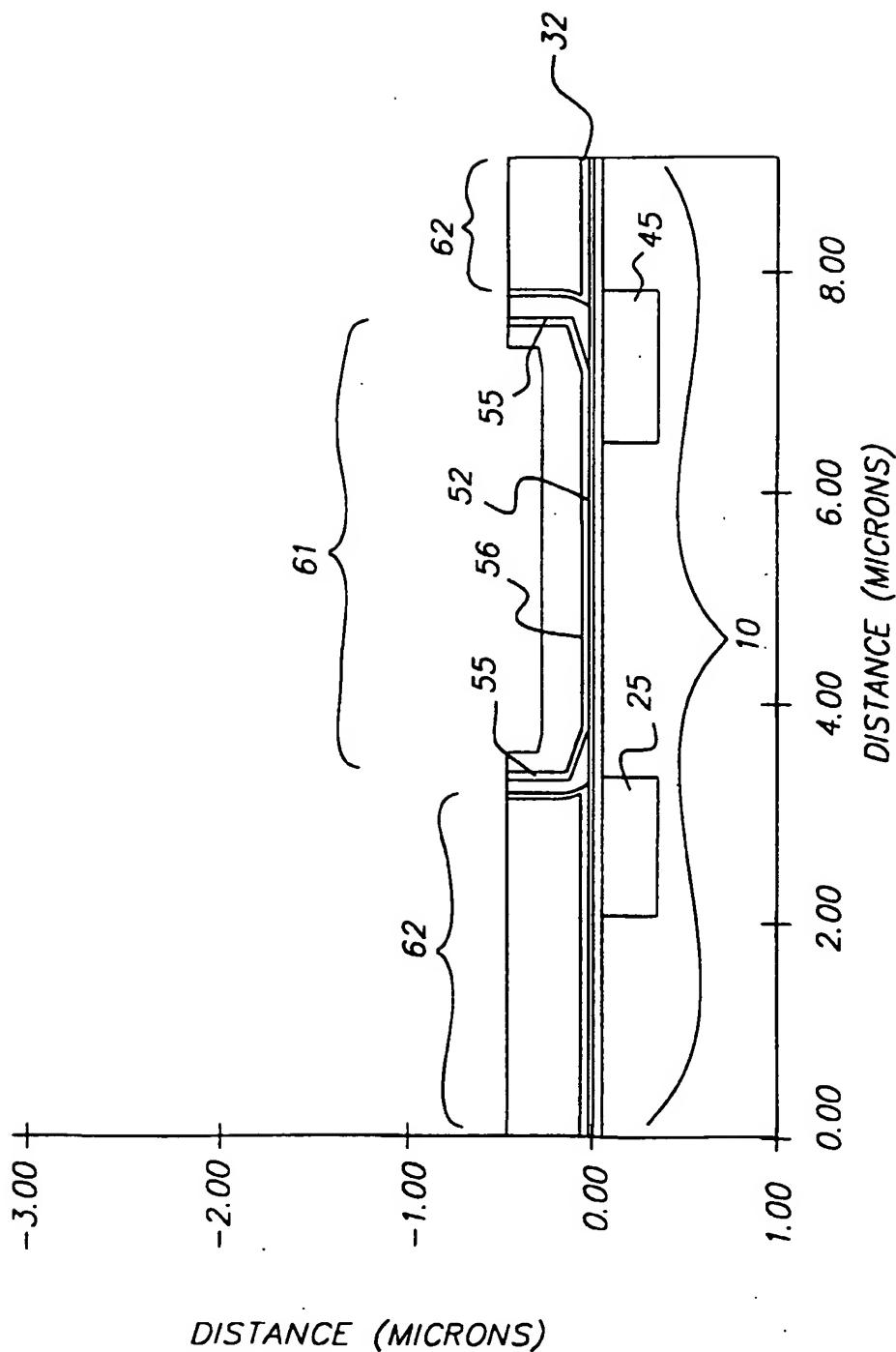


FIG. 2i

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(54) Charge coupled image sensor with u-shaped gates

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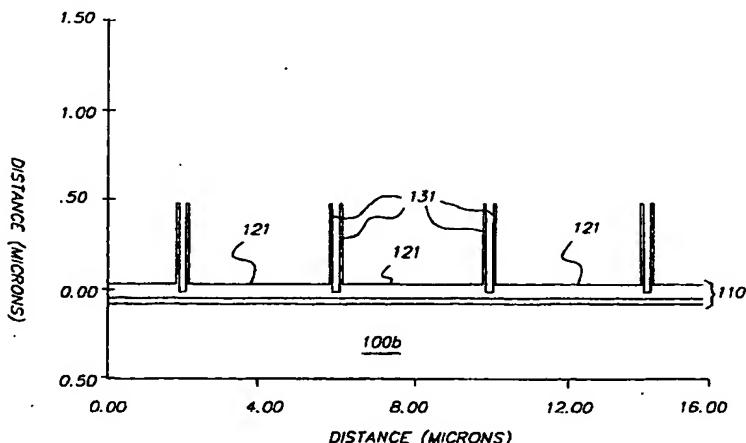


FIG. 1c



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 00 20 3873

DOCUMENTS CONSIDERED TO BE RELEVANT														
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl7)											
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A	US 5 029 321 A (KIMURA MIKIHIRO) 2 July 1991 (1991-07-02) * the whole document *	1-10												

TECHNICAL FIELDS SEARCHED (Int.Cl7)														
H01L														
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>The Hague</td> <td>8 July 2004</td> <td>Boero, M</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	The Hague	8 July 2004	Boero, M					
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<p>CATEGORY OF CITED DOCUMENTS</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">X : particularly relevant if taken alone</td> <td style="width: 33%;">T : theory or principle underlying the invention</td> </tr> <tr> <td>Y : particularly relevant if combined with another document of the same category</td> <td>E : earlier patent document, but published on, or after the filing date</td> </tr> <tr> <td>A : technological background</td> <td>D : document cited in the application</td> </tr> <tr> <td>O : non-written disclosure</td> <td>L : document cited for other reasons</td> </tr> <tr> <td>P : intermediate document</td> <td colspan="2" style="border-top: none;">& : member of the same patent family, corresponding document</td> </tr> </table>				X : particularly relevant if taken alone	T : theory or principle underlying the invention	Y : particularly relevant if combined with another document of the same category	E : earlier patent document, but published on, or after the filing date	A : technological background	D : document cited in the application	O : non-written disclosure	L : document cited for other reasons	P : intermediate document	& : member of the same patent family, corresponding document	
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ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 00 20 3873

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